What is Claimed is:

1. A bit error rate tester that tests the bit error rate of an interface, the bit error rate tester comprising:

a first memory storing test data;

a second memory storing comparison data;

transmission circuitry implemented using programmable logic circuitry of a programmable logic device, the transmission circuitry coupled to the interface and to the first memory for communicating the test data to the interface; and

comparison circuitry implemented using programmable logic circuitry of the programmable logic device, the comparison circuitry coupled to the interface and to the second memory for receiving incoming data from the interface and comparing the incoming data to the comparison data.

2. The bit error rate tester of claim 1 further comprising control circuitry coupled to the transmission circuitry and to the comparison circuitry.

3. The bit error rate tester of claim 2 wherein the control circuitry is implemented in the programmable logic device using programmable logic circuitry.

4. The bit error rate tester of claim 3 wherein the control circuitry is a processor.

5. The bit error rate tester of claim 1 further comprising user equipment coupled to the programmable logic device.

6. The bit error rate tester of claim 5 wherein the user equipment comprises a personal computer.

7. The bit error rate tester of claim 1 wherein the transmission circuitry comprises formatting circuitry.

8. The bit error rate tester of claim 1 wherein the comparison circuitry comprises formatting circuitry.

9. The bit error rate tester of claim 1 wherein the interface is internal to the programmable logic device.

10. The bit error rate tester of claim 1 wherein the interface is external to the programmable logic device.

11. The bit error rate tester of claim 1 wherein the first memory and the second memory are the same.

12. The bit error rate tester of claim 1 wherein the test data and the comparison data are the same.

13. A programmable logic device comprising programmable logic circuitry configured to:

communicate test data to an interface;

receive incoming data from the interface;

compare the incoming data to comparison

data in order to determine the bit error rate of the interface.

14. A programmable logic device comprising programmable logic circuitry configured to implement a bit error rate tester.

15. A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

16. The printed circuit board of claim 15 further comprising a memory mounted on the printed circuit board and coupled to the memory circuitry.

17. The printed circuit board of claim 16 further comprising processing circuitry mounted on the printed circuit board and couple to the memory circuitry.

18. A method for synchronizing a comparison of incoming values with comparison values in a bit error rate tester implemented in a programmable logic device, the method comprising:

(1) comparing an incoming value to a comparison value corresponding to an address counter;

(2) if the incoming value matches the comparison value then increasing the address counter by one unit, otherwise increasing the address counter by two units; and

(3) repeating (1) and (2) until a predetermined condition is met.

19. The method of claim 18 wherein (3) comprises repeating (1) and (2) until a predetermined number of consecutive matches have occurred.

20. The method of claim 18 wherein the comparison values comprises a pattern of values and wherein (3) comprises repeating (1) and (2) until all values in the pattern of values are consecutively matched.

21. The method of claim 18 further comprising:

when the predetermined condition is met:

(1) comparing an incoming value to a comparison value corresponding to a second address counter;

(2) increasing the second address counter by one unit and if the incoming value does not match the comparison value then increasing a bit error counter by one; and

(3) repeating (1) and (2) until a predetermined condition is met.

22. A method for testing the bit error rate of an interface using a bit error rate tester implemented in a programmable logic device, the method comprising:

communicating test data to the interface;

receiving incoming data from the interface;

comparing the incoming data to

comparison data in order to determine the bit error rate of the interface.

23. The method of claim 22 wherein the communicating test data to the interface comprises communicating test data to the interface located within the programmable logic device.

24. The method of claim 22 wherein the communicating test data to the interface comprises communicating test data the interface located outside of the programmable logic device.

25. The method of claim 22 wherein the comparing the incoming data to the comparison data comprises synchronizing the incoming data to the comparison data.